PATENT ABSTRACTS OF JAPAN

(11)Publication number : **11-054609**

(43)Date of publication of application : **26.02.1999**

(51)Int.Cl. H01L 21/76
H01L 29/78

(21)Application number : **09-223041**

(22)Date of filing : **05.08.1997**

(71)Applicant : **NIPPON STEEL CORP**

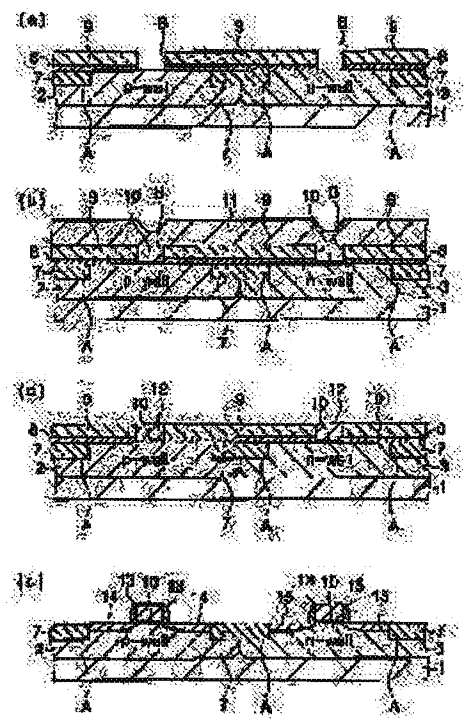
(72)Inventor : **KUMAZAKI YOSHIHIRO**

(54) METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To enable ensuring device isolation by planarizing an embedded oxide film in a device isolation region and preventing etching residue at embedded gate wiring forming, in a method for forming embedded gate wiring.

SOLUTION: After a trench for shallow trench isolation A has been formed on a semiconductor substrate 1, a silicon oxide film is formed and then only a silicon oxide film 7 is left in the trench A by filling a silicon oxide film in the trench A and polishing it. Next, after a thermal oxide film 8 and a silicon nitride film 9 have been sequentially deposited on the semiconductor substrate 1, an aperture B is opened on the silicon nitride film 9 for a gate electrode forming region and then a polysilicon film 11 is formed so as to embed the aperture B. Subsequently, the polysilicon film 11 is polished until the silicon nitride film 9 is exposed, a gate electrode made of the polysilicon film 11 is formed in the aperture B, and then the silicon nitride film 9 is removed.



* NOTICES *

CLAIMS

[Claim(s)]

[Claim 1]A manufacturing method of a semiconductor device characterized by comprising the following.
The 1st process of depositing the 1st oxide film on said semiconductor substrate so that said Mizouchi may be embedded after forming a slot in a semiconductor substrate.
The 2nd process of grinding said 1st oxide film until said semiconductor substrate surface is exposed.
The 3rd process of forming an opening in said nitride by patterning said nitride after forming the 2nd oxide film and a nitride one by one on said semiconductor substrate.
The 4th process of giving thermal oxidation to said semiconductor substrate and forming an oxidizing film in said semiconductor substrate surface under said opening, the 5th process of forming a silicon film all over said semiconductor substrate top so that said opening may be embedded, and the 6th process of grinding said silicon film until said nitride is exposed.

[Claim 2]A manufacturing method of a semiconductor device characterized by comprising the following.
The 1st process of depositing an oxide film on said semiconductor substrate so that said Mizouchi may be embedded after forming a slot in a semiconductor substrate.
The 2nd process of giving thermal oxidation to said semiconductor substrate and forming an oxidizing film in said semiconductor substrate surface under said opening after forming an opening in said oxide film.
The 3rd process of forming a silicon film on said semiconductor substrate so that inside of said opening may be embedded.
The 4th process of grinding said silicon film until said oxide film is exposed.

[Claim 3]A manufacturing method of a semiconductor device providing further the 7th process of removing said nitride in a manufacturing method of the semiconductor device according to claim 1 by wet etching which used a heat phosphoric acid solution after said 6th process.
[Claim 4]A manufacturing method of a semiconductor device, wherein said 4th process includes a process of grinding said oxide film and carrying out flattening of said oxide film surface, in a manufacturing method of the semiconductor device according to claim 2.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]Especially this invention relates to the formation method of the gate wire of a MOS transistor about the manufacturing method of a semiconductor device.
[0002]
[Description of the Prior Art]About the formation method of the conventional gate wire, it is indicated by JP,6-29530,A, JP,7-240519,A, etc., for example. The field oxide by LOCOS process is used for the isolation region of said prior patent.
[0003]In order to form a detailed gate wire in said JP,7-240519,A, after forming the field oxide for isolation in a semiconductor substrate, an oxidizing film is formed in an element active region by a thermal oxidation method, and the silicon nitride film is formed on this oxidizing film.
[0004]Next, an opening is formed in the resist film of the field which applies photoresist on said silicon nitride film, next forms a gate electrode. Then, the silicon nitride film and oxidizing film under said opening are etched one by one by using photoresist as a mask, and the silicon nitride film under an opening and silicon oxide are removed.
[0005]Next, after forming an oxidizing film in the semiconductor substrate surface under an opening and forming a polycrystalline silicon film on this oxidizing film by giving thermal oxidation to a semiconductor substrate after removing a photoresist film, whole surface etchback of this polycrystalline silicon film is carried out. This etchback removes thoroughly the polycrystalline silicon film formed on the silicon nitride film, and makes a polycrystalline silicon film remain only in an opening. This polycrystalline silicon film serves as a gate electrode. Then, etchback of the silicon nitride film is carried out, and it is removed. After an appropriate time, a gate electrode is used as a mask, an ion implantation is carried out, and a source drain area is formed in the surface of the semiconductor substrate of gate electrode both sides.
[0006]
[Problem(s) to be Solved by the Invention]However, in the formation method of the gate wire using the isolation technique by the conventional LOCOS process. The silicon nitride film and oxidizing film under said opening are etched one by one by using photoresist as a mask, Even after removing the silicon nitride film under an opening, and silicon oxide, it is easy to produce the etching residue of a silicon nitride film in the border area (LOCOS step part) of an element activity (active) field and an isolation (field) field. The more the level difference of an active region and an isolation region is large, the more a silicon nitride film remains easily.
[0007]This is because an anisotropic-dry-etching method must be used in order to raise working shape and dimensional accuracy, when etching a silicon nitride film. Then, if the amount of over etching is increased in order to prevent the etching residue of a silicon nitride film, the field oxide itself formed with LOCOS process will be etched, and the LOCOS thickness directly under a gate wire will become thinner than predetermined thickness. As a result, the threshold of a parasitic transistor is reduced and the problem of stopping being able to carry out isolation electrically arises.
[0008]The purpose of this invention aims at preventing the etch residue at the time of embedding gate wire formation, and enabling it to perform isolation certainly by [of the embedded oxide film of an isolation region] carrying out flattening in an embedding gate wire formation method.
[0009]
[Means for Solving the Problem]A manufacturing method of the 1st semiconductor device of this invention is provided with the following.
The 1st process of depositing the 1st oxide film on said semiconductor substrate so that said Mizouchi may be

embedded after forming a slot in a semiconductor substrate.
The 2nd process of grinding said 1st oxide film until said semiconductor substrate surface is exposed.
The 3rd process of forming an opening in said nitride by patterning said nitride after forming the 2nd oxide film and a nitride one by one on said semiconductor substrate.
The 4th process of giving thermal oxidation to said semiconductor substrate and forming an oxidizing film in said semiconductor substrate surface under said opening, the 5th process of forming a silicon film all over said semiconductor substrate top so that said opening may be embedded, and the 6th process of grinding said silicon film until said nitride is exposed.

[0010]A manufacturing method of the 1st semiconductor device of this invention possesses further the 7th process of removing said nitride by wet etching which used a heat phosphoric acid solution after said 6th process.
[0011]A manufacturing method of the 2nd semiconductor device of this invention is provided with the following.
The 1st process of depositing an oxide film on said semiconductor substrate so that said Mizouchi may be embedded after forming a slot in a semiconductor substrate.
The 2nd process of giving thermal oxidation to said semiconductor substrate and forming an oxidizing film in said semiconductor substrate surface under said opening after forming an opening in said oxide film.
The 3rd process of forming a silicon film on said semiconductor substrate so that inside of said opening may be embedded.
The 4th process of grinding said silicon film until said oxide film is exposed.

[0012]A manufacturing method of the 2nd semiconductor device of this invention possesses a process to which said 4th process grinds said oxide film, and carries out flattening of said oxide film surface.
[0013]
[Embodiment of the Invention]Below, the manufacturing method of the semiconductor device concerning a 1st embodiment of this invention is concretely explained based on drawing 1 (a) - (d) and drawing 2 (a) - (d). These drawing 1 (a) - (d) and drawing 2 (a) - (d) is manufacturing process drawings of longitudinal section showing the manufacturing method of the semiconductor device concerning a 1st embodiment of this invention.
[0014]As shown in drawing 1 (a), after forming the 4-micrometer p type well 2 and the n type well 3, it forms in the p type silicon semiconductor substrate 1, and the 50-nm-thick oxidizing film 4 is formed on the depth 3 - the semiconductor substrate 1 from a surface. After applying the resist 5 on this oxidizing film 4, this resist 5 is patterned. This patterning is patterning for forming a STI (shanowtrench isolation) isolation region.
[0015]Next, as shown in drawing 1 (b), the 0.3-0.5-micrometer-deep slot A is formed in the semiconductor substrate 1 from the semiconductor substrate 1 surface by etching the oxidizing film 4 and the semiconductor substrate 1 which were formed in the isolation region one by one by using resist 5 as a mask.
[0016]Next, as shown in drawing 1 (c), after removing the resist 5, thermal oxidation is given to the semiconductor substrate 1, and after forming the oxidizing film which is not illustrated in the slot A, the oxide film 6 about 1 micrometer thick is further formed on this oxidizing film that is not illustrated with a vacuum CVD method.
[0017]Next, by a chemical-and-mechanical-grinding (CMP) method, as shown in drawing 1 (d), the silicon oxide 6 is ground until the p type well 2 and the n type well 3 of the semiconductor substrate 1 are exposed. The element isolation structure 7 which makes the silicon oxide 6 remain and consists of the silicon oxide 6 only in the slot A by this polish is formed.
[0018]Next, as shown in drawing 2 (a), thermal oxidation is given to the semiconductor substrate 1 surface, and the oxidizing film 8 about 50 nm thick is formed in the semiconductor substrate 1 surface. Then, the silicon nitride film 9 about 300 nm thick is deposited on the oxidizing film 8 with a vacuum CVD method. Next, pattern formation of the silicon nitride film 9 is carried out with photolithography technique and etching technology. That is, it is the process of forming the opening B for gate wire 12 mentioned later.
[0019]Next, as shown in drawing 2 (b), point ** of the oxidizing film 8 formed in the field which removed the silicon nitride film 9 is carried out, and it is removed. Then, thermal oxidation is given to the semiconductor substrate 1 and the about 6-10-nm-thick gate oxide 10 is formed in semiconductor substrate 1 surface of a field which removed the oxidizing film 8. Then, the polycrystalline silicon film 11 about 0.5 micrometer thick is deposited with a vacuum CVD method on the semiconductor substrate 1 including the gate oxide 10 top. Next, phosphorus (p) is introduced into said polycrystalline silicon film 11, and conductivity is given.
[0020]Next, by the CMP method, as shown in drawing 2 (c), the gate wire 12 which consists of the polycrystalline silicon film 11 is formed by grinding the polycrystalline silicon film 11 until the surface of the silicon nitride film 9 is

exposed. That is, it is the process of forming the gate wire 12 by making the polycrystalline silicon film 11 remaining only in the opening B.
[0021]Next, as shown in drawing 2 (d), the wet etching of a heat phosphoric acid solution removes the silicon nitride film 9. Then, in order to form the LDD region of a transistor, the ion implantation of phosphorus (P) and the boron (B) is carried out to n **CHANERU field and p **CHANERU field, respectively (not shown).
[0022]Then, after depositing the 200-nm-thick silicon oxide 13 with a vacuum CVD method, the side wall oxide film 13 which consists the semiconductor substrate 1 whole surface of the silicon oxide 13 by performing dry etching of anisotropy is formed. The source drain area 14 of the transistor of an n-type channel and the source drain area 15 of the transistor of a p type channel are formed by performing a publicly known ion implantation and heat treatment after that.
[0023]Next, the manufacturing method of the semiconductor device concerning a 2nd embodiment of this invention is explained based on drawing 1 (a) - (c) and drawing 3 (a) - (d). Drawing 3 is manufacturing process drawing of longitudinal section showing the manufacturing method of the semiconductor device concerning a 2nd embodiment of this invention. After the process shown in drawing 1 [of a 1st embodiment mentioned above] (a) - (c), as shown in drawing 3 (a), the slot 16 for gate wires is formed with photolithography technique and etching technology at the silicon oxide 6.
[0024]Next, the oxide film 6 of the pars basilaris ossis occipitalis of this slot 16 is washed and removed. as a result, this p -- the well 2 and n -- each bottom of the two slots 16 in which the field of the well 3 was formed independently serves as semiconductor substrate 1 surface of the element formation region on the p type well 2 and the n type well 3. Then, thermal oxidation is given to the semiconductor substrate 1 and the about 6-10-nm-thick gate oxide 10 is formed in semiconductor substrate 1 surface of slot 16 pars basilaris ossis occipitalis.
[0025]Next, as shown in drawing 3 (b), the polycrystalline silicon film 11 about 0.5 micrometer thick is deposited with a vacuum CVD method on the semiconductor substrate 1 including the gate oxide 10 top. Next, phosphorus (p) is introduced into the polycrystalline silicon film 11, and conductivity is given.
[0026]Then, as shown in drawing 3 (c), the gate wire 12 which consists of the polycrystalline silicon film 11 by the CMP method by grinding simultaneously the polycrystalline silicon film 11 and the silicon oxide 6 is formed, and flattening of the surface of the silicon oxide 6 is carried out. It is made for the thickness of the polycrystalline silicon film 11 embedded in the slot 16 to be set to 0.2-0.4 micrometer.
[0027]Next, as shown in drawing 3 (d), all over semiconductor substrate 1, by [of anisotropy] carrying out dry etching, the silicon oxide 6 is made to remain in the slot A, and the element isolation structure 7 which consists of the silicon oxide 6 is formed by this etching. Then, in order to form the LDD region of a transistor, the ion implantation of phosphorus (P) and the boron (B) is carried out to n **CHANERU field and p **CHANERU field, respectively (not shown).
[0028]Then, after depositing the 200-nm-thick silicon oxide 13 with a vacuum CVD method, the side wall oxide film 13 which consists of the silicon oxide 13 is formed by performing dry etching of anisotropy all over semiconductor substrate 1.
[0029]The source drain area 14 of the transistor of an n-type channel and the source drain area 15 of the transistor of a p type channel are formed by performing a publicly known ion implantation and heat treatment after that.
[0030]After the manufacturing method of the semiconductor device concerning a 1st embodiment of this invention forms the shallow slot A for trench isolation in the semiconductor substrate 1, it forms the silicon oxide 6 all over semiconductor substrate 1, and is filled up with the silicon oxide 6 in the slot A.
[0031]Then, the silicon oxide 6 is ground with chemical machinery grinding method (CMP). This polish is performed until the surface of the semiconductor substrate 1 is exposed, and it makes the silicon oxide 7 remain only in the slot A.
[0032]Then, after forming the opening B in the silicon nitride film 9 which serves as a formation area of a gate electrode after depositing the oxidizing film 8 and the silicon nitride film 9 one by one on the semiconductor substrate 1 and giving thermal oxidation all over semiconductor substrate 1, the polycrystalline silicon film 11 is deposited so that the opening B may be embedded. Next, by the CMP method, the polycrystalline silicon film 11 is ground until the silicon nitride film 9 is exposed, and gate electrode 12 shape which consists of the polycrystalline silicon film 11 is formed in the opening B.
[0033]By removing the silicon nitride film 9 by the wet etching method using a heat phosphoric acid solution after an appropriate time, Since there are no problems, such as an etch residue of the silicon nitride film in the step part of the element active region (active region) and field region like before, by using the shallow trench separation

method for the isolation technique, the etching residue at the time of Oba etching of a silicon nitride film does not arise. Therefore, the threshold of the Field transistor formed parasitically is not reduced. Variation in gate wire width is not produced and abnormalities, such as vena contracta of sectional shape or a taper, are not produced, either.

[0034]The manufacturing method of the semiconductor device concerning a 2nd embodiment forms the slot used as a shallow trench separation layer in the semiconductor substrate 1. The silicon oxide 6 is formed all over semiconductor substrate 1, and Mizouchi is filled up with the silicon oxide 6. The slot 16 for gate wires is formed in the silicon oxide 6 with photolithography technique and etching technology. Then, the oxide film 6 of said slot 16 pars basilaris ossis occipitalis is washed and removed.

[0035]After forming the gate oxide 10 in semiconductor substrate 1 surface of slot 16 pars basilaris ossis occipitalis by giving thermal oxidation to the semiconductor substrate 1, the polycrystalline silicon film 11 is deposited so that an opening may be embedded. Next, by the CMP method, the polycrystalline silicon film 11 is ground until the silicon oxide 6 is exposed, and gate electrode 12 shape which consists of the polycrystalline silicon film 11 is formed in an opening. Then, the element isolation structure 7 which consists of the silicon oxide 6 is formed by carrying out etchback of the silicon oxide. Next, the etching residue at the time of Oba etching of a silicon nitride film does not arise by using the shallow trench separation method for the isolation technique.

[0036]Therefore, the threshold of the Field transistor formed parasitically is not reduced. The variation in gate wire width does not arise and abnormalities, such as vena contracta of sectional shape or a taper, are not produced, either. Since an embedding gate wire is formed and the element isolation structure 7 is formed using the silicon oxide 6, it becomes possible to simplify the manufacturing process number of embedding gate wire formation.

[0037]

[Effect of the Invention]As explained above, according to this invention, in embedding gate wire formation, it becomes possible by carrying out flattening of the trench type embedded oxide film to lose the wiring short by wiring etching residue, and an etching damage, and to form a gate wire with sufficient dimensional accuracy.

[Translation done.]

* NOTICES *

TECHNICAL FIELD

[Field of the Invention]Especially this invention relates to the formation method of the gate wire of a MOS transistor about the manufacturing method of a semiconductor device.

[Translation done.]

* NOTICES *

JPO and INPIT are not responsible for any damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

PRIOR ART

[Description of the Prior Art]About the formation method of the conventional gate wire, it is indicated by JP,6-29530,A, JP,7-240519,A, etc., for example. The field oxide by LOCOS process is used for the isolation region of said prior patent.
[0003]In order to form a detailed gate wire in said JP,7-240519,A, after forming the field oxide for isolation in a semiconductor substrate, an oxidizing film is formed in an element active region by a thermal oxidation method, and the silicon nitride film is formed on this oxidizing film.
[0004]Next, an opening is formed in the resist film of the field which applies photoresist on said silicon nitride film, next forms a gate electrode. Then, the silicon nitride film and oxidizing film under said opening are etched one by one by using photoresist as a mask, and the silicon nitride film under an opening and silicon oxide are removed.
[0005]Next, after forming an oxidizing film in the semiconductor substrate surface under an opening and forming a polycrystalline silicon film on this oxidizing film by giving thermal oxidation to a semiconductor substrate after removing a photoresist film, whole surface etchback of this polycrystalline silicon film is carried out. This etchback removes thoroughly the polycrystalline silicon film formed on the silicon nitride film, and makes a polycrystalline silicon film remain only in an opening. This polycrystalline silicon film serves as a gate electrode. Then, etchback of the silicon nitride film is carried out, and it is removed. After an appropriate time, a gate electrode is used as a mask, an ion implantation is carried out, and a source drain area is formed in the surface of the semiconductor substrate of gate electrode both sides.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention]As explained above, in this invention, flattening of the trench type embedded oxide film is carried out in embedding gate wire formation.
Therefore, it becomes possible to lose the wiring short by wiring etching residue, and an etching damage, and to form a gate wire with sufficient dimensional accuracy.

[Translation done.]

* NOTICES *

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]However, in the formation method of the gate wire using the isolation technique by the conventional LOCOS process. The silicon nitride film and oxidizing film under said opening are etched one by one by using photoresist as a mask, Even after removing the silicon nitride film under an opening, and silicon oxide, it is easy to produce the etching residue of a silicon nitride film in the border area (LOCOS step part) of an element activity (active) field and an isolation (field) field. The more the level difference of an active region and an isolation region is large, the more a silicon nitride film remains easily.
[0007]This is because an anisotropic-dry-etching method must be used in order to raise working shape and dimensional accuracy, when etching a silicon nitride film. Then, if the amount of over etching is increased in order to prevent the etching residue of a silicon nitride film, the field oxide itself formed with LOCOS process will be etched, and the LOCOS thickness directly under a gate wire will become thinner than predetermined thickness. As a result, the threshold of a parasitic transistor is reduced and the problem of stopping being able to carry out isolation electrically arises.
[0008]The purpose of this invention aims at preventing the etch residue at the time of embedding gate wire formation, and enabling it to perform isolation certainly by [of the embedded oxide film of an isolation region] carrying out flattening in an embedding gate wire formation method.

[Translation done.]

MEANS

[Means for Solving the Problem]A manufacturing method of the 1st semiconductor device of this invention is provided with the following.
The 1st process of depositing the 1st oxide film on said semiconductor substrate so that said Mizouchi may be embedded after forming a slot in a semiconductor substrate.
The 2nd process of grinding said 1st oxide film until said semiconductor substrate surface is exposed.
The 3rd process of forming an opening in said nitride by patterning said nitride after forming the 2nd oxide film and a nitride one by one on said semiconductor substrate.
The 4th process of giving thermal oxidation to said semiconductor substrate and forming an oxidizing film in said semiconductor substrate surface under said opening, the 5th process of forming a silicon film all over said semiconductor substrate top so that said opening may be embedded, and the 6th process of grinding said silicon film until said nitride is exposed.

[0010]A manufacturing method of the 1st semiconductor device of this invention possesses further the 7th process of removing said nitride by wet etching which used a heat phosphoric acid solution after said 6th process.
[0011]A manufacturing method of the 2nd semiconductor device of this invention is provided with the following.
The 1st process of depositing an oxide film on said semiconductor substrate so that said Mizouchi may be embedded after forming a slot in a semiconductor substrate.
The 2nd process of giving thermal oxidation to said semiconductor substrate and forming an oxidizing film in said semiconductor substrate surface under said opening after forming an opening in said oxide film.
The 3rd process of forming a silicon film on said semiconductor substrate so that inside of said opening may be embedded.
The 4th process of grinding said silicon film until said oxide film is exposed.

[0012]A manufacturing method of the 2nd semiconductor device of this invention possesses a process to which said 4th process grinds said oxide film, and carries out flattening of said oxide film surface.
[0013]
[Embodiment of the Invention]Below, the manufacturing method of the semiconductor device concerning a 1st embodiment of this invention is concretely explained based on drawing 1 (a) - (d) and drawing 2 (a) - (d). These drawing 1 (a) - (d) and drawing 2 (a) - (d) is manufacturing process drawings of longitudinal section showing the manufacturing method of the semiconductor device concerning a 1st embodiment of this invention.
[0014]As shown in drawing 1 (a), after forming the 4-micrometer p type well 2 and the n type well 3, it forms in the p type silicon semiconductor substrate 1, and the 50-nm-thick oxidizing film 4 is formed on the depth 3 - the semiconductor substrate 1 from a surface. After applying the resist 5 on this oxidizing film 4, this resist 5 is patterned. This patterning is patterning for forming a STI (shanowtrench isolation) isolation region.
[0015]Next, as shown in drawing 1 (b), the 0.3-0.5-micrometer-deep slot A is formed in the semiconductor substrate 1 from the semiconductor substrate 1 surface by etching the oxidizing film 4 and the semiconductor substrate 1 which were formed in the isolation region one by one by using resist 5 as a mask.
[0016]Next, as shown in drawing 1 (c), after removing the resist 5, thermal oxidation is given to the semiconductor substrate 1, and after forming the oxidizing film which is not illustrated in the slot A, the oxide film 6 about 1 micrometer thick is further formed on this oxidizing film that is not illustrated with a vacuum CVD method.
[0017]Next, by a chemical-and-mechanical-grinding (CMP) method, as shown in drawing 1 (d), the silicon oxide 6 is ground until the p type well 2 and the n type well 3 of the semiconductor substrate 1 are exposed. The element

isolation structure 7 which makes the silicon oxide 6 remain and consists of the silicon oxide 6 only in the slot A by this polish is formed.
[0018]Next, as shown in drawing 2 (a), thermal oxidation is given to the semiconductor substrate 1 surface, and the oxidizing film 8 about 50 nm thick is formed in the semiconductor substrate 1 surface. Then, the silicon nitride film 9 about 300 nm thick is deposited on the oxidizing film 8 with a vacuum CVD method. Next, pattern formation of the silicon nitride film 9 is carried out with photolithography technique and etching technology. That is, it is the process of forming the opening B for gate wire 12 mentioned later.
[0019]Next, as shown in drawing 2 (b), point ** of the oxidizing film 8 formed in the field which removed the silicon nitride film 9 is carried out, and it is removed. Then, thermal oxidation is given to the semiconductor substrate 1 and the about 6-10-nm-thick gate oxide 10 is formed in semiconductor substrate 1 surface of a field which removed the oxidizing film 8. Then, the polycrystalline silicon film 11 about 0.5 micrometer thick is deposited with a vacuum CVD method on the semiconductor substrate 1 including the gate oxide 10 top. Next, phosphorus (p) is introduced into said polycrystalline silicon film 11, and conductivity is given.
[0020]Next, by the CMP method, as shown in drawing 2 (c), the gate wire 12 which consists of the polycrystalline silicon film 11 is formed by grinding the polycrystalline silicon film 11 until the surface of the silicon nitride film 9 is exposed. That is, it is the process of forming the gate wire 12 by making the polycrystalline silicon film 11 remaining only in the opening B.
[0021]Next, as shown in drawing 2 (d), the wet etching of a heat phosphoric acid solution removes the silicon nitride film 9. Then, in order to form the LDD region of a transistor, the ion implantation of phosphorus (P) and the boron (B) is carried out to n **CHANERU field and p **CHANERU field, respectively (not shown).
[0022]Then, after depositing the 200-nm-thick silicon oxide 13 with a vacuum CVD method, the side wall oxide film 13 which consists the semiconductor substrate 1 whole surface of the silicon oxide 13 by performing dry etching of anisotropy is formed. The source drain area 14 of the transistor of an n-type channel and the source drain area 15 of the transistor of a p type channel are formed by performing a publicly known ion implantation and heat treatment after that.
[0023]Next, the manufacturing method of the semiconductor device concerning a 2nd embodiment of this invention is explained based on drawing 1 (a) - (c) and drawing 3 (a) - (d). Drawing 3 is manufacturing process drawing of longitudinal section showing the manufacturing method of the semiconductor device concerning a 2nd embodiment of this invention. After the process shown in drawing 1 [of a 1st embodiment mentioned above] (a) - (c), as shown in drawing 3 (a), the slot 16 for gate wires is formed with photolithography technique and etching technology at the silicon oxide 6.
[0024]Next, the oxide film 6 of the pars basilaris ossis occipitalis of this slot 16 is washed and removed. as a result, this p -- the well 2 and n -- each bottom of the two slots 16 in which the field of the well 3 was formed independently serves as semiconductor substrate 1 surface of the element formation region on the p type well 2 and the n type well 3. Then, thermal oxidation is given to the semiconductor substrate 1 and the about 6-10-nm-thick gate oxide 10 is formed in semiconductor substrate 1 surface of slot 16 pars basilaris ossis occipitalis.
[0025]Next, as shown in drawing 3 (b), the polycrystalline silicon film 11 about 0.5 micrometer thick is deposited with a vacuum CVD method on the semiconductor substrate 1 including the gate oxide 10 top. Next, phosphorus (p) is introduced into the polycrystalline silicon film 11, and conductivity is given.
[0026]Then, as shown in drawing 3 (c), the gate wire 12 which consists of the polycrystalline silicon film 11 by the CMP method by grinding simultaneously the polycrystalline silicon film 11 and the silicon oxide 6 is formed, and flattening of the surface of the silicon oxide 6 is carried out. It is made for the thickness of the polycrystalline silicon film 11 embedded in the slot 16 to be set to 0.2-0.4 micrometer.
[0027]Next, as shown in drawing 3 (d), all over semiconductor substrate 1, by [of anisotropy] carrying out dry etching, the silicon oxide 6 is made to remain in the slot A, and the element isolation structure 7 which consists of the silicon oxide 6 is formed by this etching. Then, in order to form the LDD region of a transistor, the ion implantation of phosphorus (P) and the boron (B) is carried out to n **CHANERU field and p **CHANERU field, respectively (not shown).
[0028]Then, after depositing the 200-nm-thick silicon oxide 13 with a vacuum CVD method, the side wall oxide film 13 which consists of the silicon oxide 13 is formed by performing dry etching of anisotropy all over semiconductor substrate 1.
[0029]The source drain area 14 of the transistor of an n-type channel and the source drain area 15 of the transistor of a p type channel are formed by performing a publicly known ion implantation and heat treatment after that.

[0030]After the manufacturing method of the semiconductor device concerning a 1st embodiment of this invention forms the shallow slot A for trench isolation in the semiconductor substrate 1, it forms the silicon oxide 6 all over semiconductor substrate 1, and is filled up with the silicon oxide 6 in the slot A.
[0031]Then, the silicon oxide 6 is ground with chemical machinery grinding method (CMP). This polish is performed until the surface of the semiconductor substrate 1 is exposed, and it makes the silicon oxide 7 remain only in the slot A.
[0032]Then, after forming the opening B in the silicon nitride film 9 which serves as a formation area of a gate electrode after depositing the oxidizing film 8 and the silicon nitride film 9 one by one on the semiconductor substrate 1 and giving thermal oxidation all over semiconductor substrate 1, the polycrystalline silicon film 11 is deposited so that the opening B may be embedded. Next, by the CMP method, the polycrystalline silicon film 11 is ground until the silicon nitride film 9 is exposed, and gate electrode 12 shape which consists of the polycrystalline silicon film 11 is formed in the opening B.
[0033]By removing the silicon nitride film 9 by the wet etching method using a heat phosphoric acid solution after an appropriate time, Since there are no problems, such as an etch residue of the silicon nitride film in the step part of the element active region (active region) and field region like before, by using the shallow trench separation method for the isolation technique, the etching residue at the time of Oba etching of a silicon nitride film does not arise. Therefore, the threshold of the Field transistor formed parasitically is not reduced. Variation in gate wire width is not produced and abnormalities, such as vena contracta of sectional shape or a taper, are not produced, either.
[0034]The manufacturing method of the semiconductor device concerning a 2nd embodiment forms the slot used as a shallow trench separation layer in the semiconductor substrate 1. The silicon oxide 6 is formed all over semiconductor substrate 1, and Mizouchi is filled up with the silicon oxide 6. The slot 16 for gate wires is formed in the silicon oxide 6 with photolithography technique and etching technology. Then, the oxide film 6 of said slot 16 pars basilaris ossis occipitalis is washed and removed.
[0035]After forming the gate oxide 10 in semiconductor substrate 1 surface of slot 16 pars basilaris ossis occipitalis by giving thermal oxidation to the semiconductor substrate 1, the polycrystalline silicon film 11 is deposited so that an opening may be embedded. Next, by the CMP method, the polycrystalline silicon film 11 is ground until the silicon oxide 6 is exposed, and gate electrode 12 shape which consists of the polycrystalline silicon film 11 is formed in an opening. Then, the element isolation structure 7 which consists of the silicon oxide 6 is formed by carrying out etchback of the silicon oxide. Next, the etching residue at the time of Oba etching of a silicon nitride film does not arise by using the shallow trench separation method for the isolation technique.
[0036]Therefore, the threshold of the Field transistor formed parasitically is not reduced. The variation in gate wire width does not arise and abnormalities, such as vena contracta of sectional shape or a taper, are not produced, either. Since an embedding gate wire is formed and the element isolation structure 7 is formed using the silicon oxide 6, it becomes possible to simplify the manufacturing process number of embedding gate wire formation.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is manufacturing process drawing of longitudinal section showing the manufacturing method of the semiconductor device concerning a 1st embodiment of this invention.
[Drawing 2]It is manufacturing process drawing of longitudinal section showing the manufacturing method of the semiconductor device concerning a 1st embodiment of this invention.
[Drawing 3]It is manufacturing process drawing of longitudinal section showing the manufacturing method of the semiconductor device concerning a 2nd embodiment of this invention.
[Description of Notations]
1 Semiconductor substrate
2 P type well
3 N type well
4 Oxidizing film
5 Resist
6, 7 silicon oxide
8 Oxidizing film
9 Silicon nitride film
10 Gate oxide
11, 12 polycrystalline silicon films
13 Side wall oxide film
14 and 15 Source drain
16 Slot

[Translation done.]

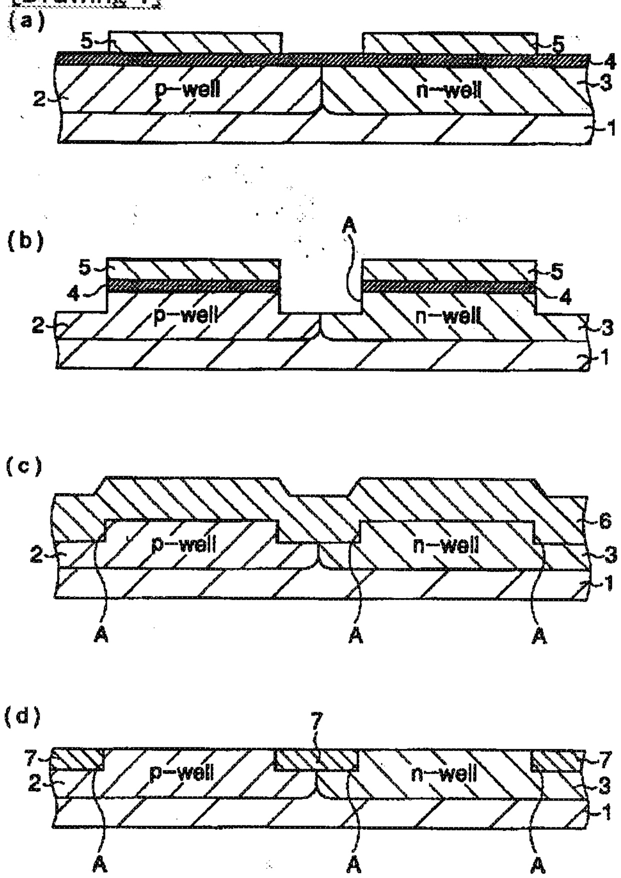
* NOTICES *

JPO and INPIT are not responsible for any damages caused by the use of this translation.

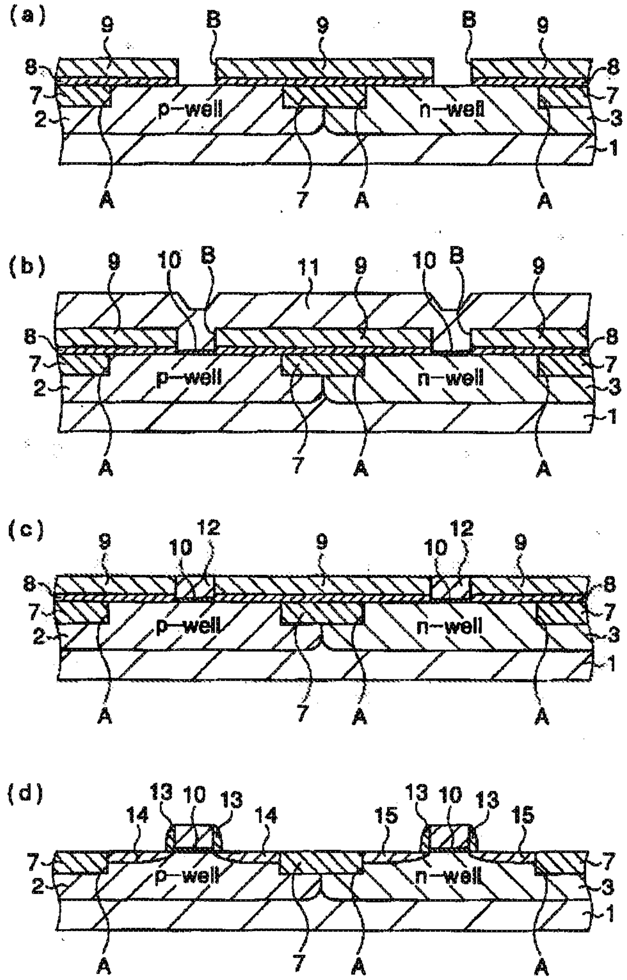
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 1]

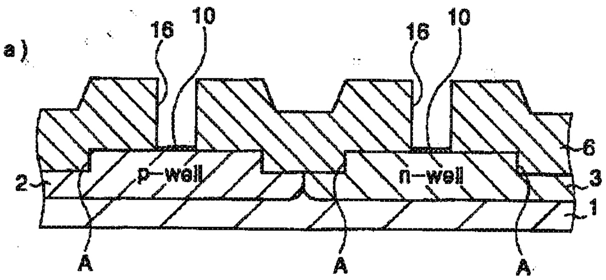


[Drawing 2]

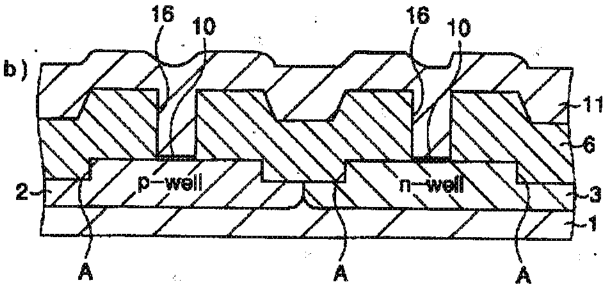


[Drawing 3]

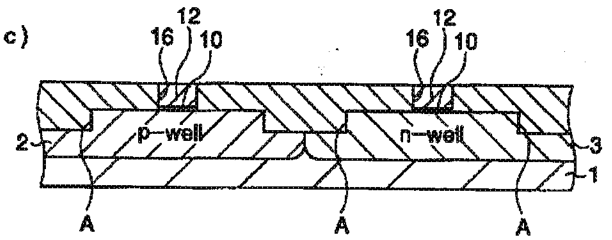
(a)



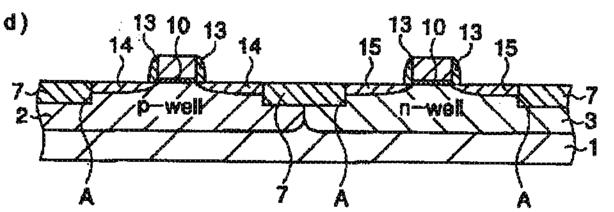
(b)



(c)



(d)



[Translation done.]

(19)日本国特許庁（ＪＰ）　(12) 公開特許公報（Ａ）　(11)特許出願公開番号

特開平11－54609

(43)公開日　平成11年(1999) 2月26日

(51)Int.Cl.[6]	識別記号	ＦＩ	
Ｈ０１Ｌ　21/76		Ｈ０１Ｌ　21/76	Ｌ
29/78		29/78	３０１Ｖ
			３０１Ｃ

審査請求　未請求　請求項の数４　ＦＤ　（全６頁）

(21)出願番号　特願平9－223041

(22)出願日　平成９年(1997) ８月５日

(71)出願人　000006655
新日本製鐵株式会社
東京都千代田区大手町２丁目６番３号

(72)発明者　熊崎　吉紘
東京都千代田区大手町２－６－３　新日本製鐵株式会社内

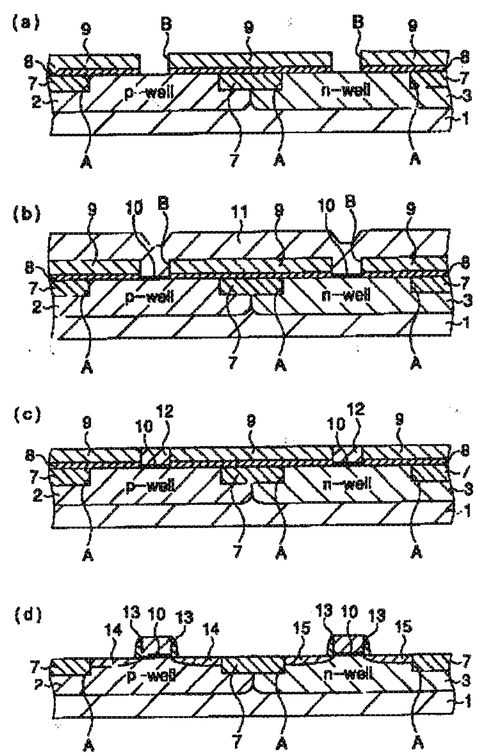
(74)代理人　弁理士　國分　孝悦

(54)【発明の名称】　半導体装置の製造方法

(57)【要約】　　（修正有）

【課題】　埋め込みゲート配線形成方法において、素子分離領域の埋め込み酸化膜を平坦化することにより、埋め込みゲート配線形成時のエッチング残渣を防止して素子分離を確実に行うことができるようにする。

【解決手段】　半導体基板１に浅いトレンチ素子分離用の溝Ａを形成した後シリコン酸化膜を形成して、前記溝Ａ内にシリコン酸化膜を充填し、その後、研磨することにより、前記溝Ａ内のみにシリコン酸化膜７を残存させる。次に、前記半導体基板１上に熱酸化膜８とシリコン窒化膜９を順次堆積した後、ゲート電極の形成領域となるシリコン窒化膜９に開口部Ｂを形成し、これを埋め込むように多結晶シリコン膜１１を堆積する。その後、シリコン窒化膜９が露出するまで多結晶シリコン膜１１を研磨して、前記開口部Ｂ内に多結晶シリコン膜１１からなるゲート電極１２形状を形成後、前記シリコン窒化膜９を除去する。



【特許請求の範囲】
【請求項1】　半導体基板に溝を形成した後、前記溝内を埋め込むように前記半導体基板上に第1の酸化膜を堆積する第1の工程と、
前記半導体基板表層が露出するまで前記第1の酸化膜を研磨する第2の工程と、
前記半導体基板上に第2の酸化膜、窒化膜を順次形成した後、前記窒化膜をパターニングすることにより、前記窒化膜に開口部を形成する第3の工程と、
前記半導体基板に熱酸化を施して、前記開口部下の前記半導体基板表層に熱酸化膜を形成する第4の工程と、
前記開口部を埋め込むように前記半導体基板上全面に珪素膜を形成する第5の工程と、
前記窒化膜が露出するまで前記珪素膜を研磨する第6の工程とを具備することを特徴とする半導体装置の製造方法。
【請求項2】　半導体基板に溝を形成した後、前記溝内を埋め込むように前記半導体基板上に酸化膜を堆積する第1の工程と、
前記酸化膜に開口部を形成した後、前記半導体基板に熱酸化を施して、前記開口部下の前記半導体基板表層に熱酸化膜を形成する第2の工程と、
前記開口部内を埋め込むように前記半導体基板上に珪素膜を形成する第3の工程と、
前記酸化膜が露出するまで前記珪素膜を研磨する第4の工程とを具備することを特徴とする半導体装置の製造方法。
【請求項3】　請求項1に記載の半導体装置の製造方法において、
前記第6の工程後に、熱燐酸溶液を用いたウエットエッチングにより前記窒化膜を除去する第7の工程を更に具備することを特徴とする半導体装置の製造方法。
【請求項4】　請求項2に記載の半導体装置の製造方法において、
前記第4の工程が、前記酸化膜を研磨して前記酸化膜表層を平坦化する工程を含むことを特徴とする半導体装置の製造方法。
【発明の詳細な説明】
【0001】
【発明の属する技術分野】本発明は、半導体装置の製造方法に関し、特に、MOS型トランジスタのゲート配線の形成方法に関するものである。
【0002】
【従来の技術】従来のゲート配線の形成方法に関しては、例えば、特開平6−29530号公報や特開平7−240519号公報などに開示されている。前記先行特許の素子分離領域は、LOCOS法によるフィールド酸化膜を用いている。
【0003】前記特開平7−240519号公報には、微細なゲート配線を形成するためには、半導体基板に素子分離用のフィールド酸化膜を形成した後、素子活性領域に熱酸化法により熱酸化膜を形成し、この熱酸化膜上にシリコン窒化膜を形成している。
【0004】次に、前記シリコン窒化膜上にフォトレジストを塗布し、次に、ゲート電極を形成する領域のレジスト膜に開口部を形成する。その後、フォトレジストをマスクとして前記開口部下のシリコン窒化膜と熱酸化膜を順次エッチングし、開口部下のシリコン窒化膜、シリコン酸化膜を除去する。
【0005】次に、フォトレジスト膜を除去した後に、半導体基板に熱酸化を施すことにより、開口部下の半導体基板表層に熱酸化膜を形成し、この熱酸化膜上に多結晶シリコン膜を形成した後、この多結晶シリコン膜を全面エッチバックする。このエッチバックは、シリコン窒化膜上に形成された多結晶シリコン膜を完全に除去し、開口部内にのみ多結晶シリコン膜を残存させる。この多結晶シリコン膜が、ゲート電極となる。その後、シリコン窒化膜をエッチバックして除去する。しかる後、ゲート電極をマスクとしてイオン注入し、ソース・ドレイン領域をゲート電極両側の半導体基板の表層に形成する。
【0006】
【発明が解決しようとする課題】しかしながら、従来のLOCOS法による素子分離手法を用いたゲート配線の形成方法では、フォトレジストをマスクとして前記開口部下のシリコン窒化膜と熱酸化膜を順次エッチングし、開口部下のシリコン窒化膜、シリコン酸化膜を除去した後も素子活性（アクティブ）領域と素子分離（フィールド）領域との境界領域（LOCOS段差部分）にシリコン窒化膜のエッチング残りが生じやすい。アクティブ領域と素子分離領域との段差が大きければ大きいほどシリコン窒化膜が残りやすくなる。
【0007】これは、シリコン窒化膜をエッチングするときに加工形状および寸法精度を向上させるために、異方性ドライエッチング法を使わざるをえないからである。そこでシリコン窒化膜のエッチング残りを防ぐために、オーバーエッチング量を増やすと、LOCOS法により形成したフィールド酸化膜そのものがエッチングされてしまい、ゲート配線直下のLOCOS膜厚が所定の膜厚よりも薄くなる。その結果、寄生トランジスタのしきい値を低下させ、電気的に素子分離できなくなるという問題が生じる。
【0008】本発明の目的は、埋め込みゲート配線形成方法において、素子分離領域の埋め込み酸化膜の平坦化することにより、埋め込みゲート配線形成時のエッチング残渣を防止して素子分離を確実に行うことができるようにすることを目的とする。
【0009】
【課題を解決するための手段】本発明の第1の半導体装置の製造方法は、半導体基板に溝を形成した後、前記溝内を埋め込むように前記半導体基板上に第1の酸化膜を

堆積する第１の工程と、前記半導体基板表層が露出するまで前記第１の酸化膜を研磨する第２の工程と、前記半導体基板上に第２の酸化膜、窒化膜を順次形成した後、前記窒化膜をパターニングすることにより、前記窒化膜に開口部を形成する第３の工程と、前記半導体基板に熱酸化を施して、前記開口部下の前記半導体基板表層に熱酸化膜を形成する第４の工程と、前記開口部を埋め込むように前記半導体基板上全面に珪素膜を形成する第５の工程と、前記窒化膜が露出するまで前記珪素膜を研磨する第６の工程とを具備する。

【００１０】また、本発明の第１の半導体装置の製造方法は、前記第６の工程後に、熱燐酸溶液を用いたウエットエッチングにより前記窒化膜を除去する第７の工程を更に具備する。

【００１１】また、本発明の第２の半導体装置の製造方法は、半導体基板に溝を形成した後、前記溝内を埋め込むように前記半導体基板上に酸化膜を堆積する第１の工程と、前記酸化膜に開口部を形成した後、前記半導体基板に熱酸化を施して、前記開口部下の前記半導体基板表層に熱酸化膜を形成する第２の工程と、前記開口部内を埋め込むように前記半導体基板上に珪素膜を形成する第３の工程と、前記酸化膜が露出するまで前記珪素膜を研磨する第４の工程とを具備する。

【００１２】また、本発明の第２の半導体装置の製造方法は、前記第４の工程が、前記酸化膜を研磨して前記酸化膜表層を平坦化する工程を具備する。

【００１３】

【発明の実施の形態】以下に、本発明の第１の実施形態に係る半導体装置の製造方法を図１（ａ）～（ｄ）、図２（ａ）～（ｄ）に基づき具体的に説明する。これらの図１（ａ）～（ｄ）、図２（ａ）～（ｄ）は、本発明の第１の実施形態に係る半導体装置の製造方法を示す製造工程縦断面図である。

【００１４】図１（ａ）に示すように、ｐ型シリコン半導体基板１に表層から深さ３～４μｍのｐ型ウエル２及びｎ型ウエル３を形成した後、半導体基板１上に厚さ５０ｎｍの熱酸化膜４を形成する。この熱酸化膜４上にレジスト５を塗布した後、このレジスト５をパターニングする。このパターニングは、ＳＴＩ（ｓｈａｎｏｗｔｒｅｎｃｈ　ｉｓｏｌａｔｉｏｎ）素子分離領域を形成するためのパターニングである。

【００１５】次に、図１（ｂ）に示すように、レジスト５をマスクとして、素子分離領域に形成された熱酸化膜４と半導体基板１を順次エッチングすることにより、半導体基板１表面から深さ０．３～０．５μｍの溝Ａを半導体基板１に形成する。

【００１６】次に、図１（ｃ）に示すように、レジスト５を除去した後、半導体基板１に熱酸化を施して、溝Ａ内に図示しない熱酸化膜を形成した後、更に、減圧ＣＶＤ法により、この図示しない熱酸化膜上に厚さ約１μｍの酸化膜６を形成する。

【００１７】次に、図１（ｄ）に示すように、化学的機械的研磨（ＣＭＰ）法により、半導体基板１のｐ型ウエル２及びｎ型ウエル３が露出するまでシリコン酸化膜６を研磨する。この研磨により、溝Ａ内にのみにシリコン酸化膜６を残存させてシリコン酸化膜６からなる素子分離構造７を形成する。

【００１８】次に、図２（ａ）に示すように、半導体基板１表面に熱酸化を施して、半導体基板１表面に厚さ約５０ｎｍの熱酸化膜８を形成する。その後、減圧ＣＶＤ法により、熱酸化膜８上に厚さ約３００ｎｍのシリコン窒化膜９を堆積する。次に、フォトリソグラフィ技術及びエッチング技術により、シリコン窒化膜９をパターン形成する。すなわち、後述するゲート配線１２用の開口部Ｂを形成する工程である。

【００１９】次に、図２（ｂ）に示すように、シリコン窒化膜９を除去した領域に形成された熱酸化膜８を先浄して除去する。その後、半導体基板１に熱酸化を施して、熱酸化膜８を除去した領域の半導体基板１表層に厚さ約６～１０ｎｍのゲート酸化膜１０を形成する。その後、減圧ＣＶＤ法により、ゲート酸化膜１０上を含む半導体基板１上に厚さ約０．５μｍの多結晶シリコン膜１１を堆積する。次に、前記多結晶シリコン膜１１に燐（ｐ）を導入し、導電性を持たせる。

【００２０】次に、図２（ｃ）に示すように、ＣＭＰ法により、シリコン窒化膜９の表層が露出するまで多結晶シリコン膜１１を研磨することにより、多結晶シリコン膜１１からなるゲート配線１２を形成する。すなわち、開口部Ｂ内のみに多結晶シリコン膜１１を残存させることにより、ゲート配線１２を形成する工程である。

【００２１】次に、図２（ｄ）に示すように、熱燐酸溶液のウエットエッチングにより、シリコン窒化膜９を除去する。その後、トランジスタのＬＤＤ領域を形成するために、ｎ‐チャネル領域、ｐ‐チャネル領域にそれぞれ燐（Ｐ）、ボロン（Ｂ）をイオン注入する（図示せず）。

【００２２】その後、減圧ＣＶＤ法により厚さ２００ｎｍのシリコン酸化膜１３を堆積した後、半導体基板１全面を異方性のドライエッチングを施すことにより、シリコン酸化膜１３からなるサイドウォール酸化膜１３を形成する。その後は、公知のイオン注入および熱処理を施すことによって、ｎ型チャネルのトランジスタのソース・ドレーン領域１４、及びｐ型チャネルのトランジスタのソース・ドレーン領域１５を形成する。

【００２３】次に、本発明の第２の実施形態に係る半導体装置の製造方法を図１（ａ）～（ｃ）、及び図３（ａ）～（ｄ）に基づき説明する。図３は、本発明の第２の実施形態に係る半導体装置の製造方法を示す製造工程縦断面図である。前述した第１の実施形態の図１（ａ）～（ｃ）に示した工程後に、図３（ａ）に示すよ

うに、フォトリソグラフィ技術及びエッチング技術により、シリコン酸化膜6にゲート配線用の溝16を形成する。

【0024】次に、この溝16の底部の酸化膜6を洗浄して除去する。その結果、このpウエル2及びnウエル3の領域の別々に形成された2つの溝16の各々の底面が、p型ウエル2及びn型ウエル3上の素子形成領域の半導体基板1表層となる。その後、半導体基板1に熱酸化を施して、溝16底部の半導体基板1表層に厚さ約6～10nmのゲート酸化膜10を形成する。

【0025】次に、図3（b）に示すように、減圧CVD法により、ゲート酸化膜10上を含む半導体基板1上に厚さ約0．5μmの多結晶シリコン膜11を堆積する。次に、多結晶シリコン膜11に燐（p）を導入し、導電性を持たせる。

【0026】この後、図3（c）に示すように、CMP法により、多結晶シリコン膜11及びシリコン酸化膜6を同時に研磨することにより、多結晶シリコン膜11からなるゲート配線12を形成すると共に、シリコン酸化膜6の表層を平坦化する。なお、溝16に埋め込まれた多結晶シリコン膜11の厚さが0．2～0．4μmになるようにする。

【0027】次に、図3（d）に示すように、半導体基板1全面に異方性のドライエッチングすることにより、シリコン酸化膜6を溝A内に残存させ、このエッチングにより、シリコン酸化膜6からなる素子分離構造7を形成する。その後、トランジスタのLDD領域を形成するために、n-チャネル領域、p-チャネル領域にそれぞれ燐（P）、ボロン（B）をイオン注入する（図示せず）。

【0028】その後、減圧CVD法により厚さ200nmのシリコン酸化膜13を堆積した後、半導体基板1全面に異方性のドライエッチングを施すことにより、シリコン酸化膜13からなるサイドウォール酸化膜13を形成する。

【0029】その後は、公知のイオン注入および熱処理を施すことによって、n型チャネルのトランジスタのソース・ドレーン領域14、及びp型チャネルのトランジスタのソース・ドレーン領域15を形成する。

【0030】本発明の第1の実施形態に係る半導体装置の製造方法は、半導体基板1に浅いトレンチ素子分離用の溝Aを形成した後、半導体基板1全面にシリコン酸化膜6を形成して、溝A内にシリコン酸化膜6を充填する。

【0031】その後、化学機械研磨法（CMP）により、シリコン酸化膜6を研磨する。この研磨は、半導体基板1の表層が露出するまで行い、溝A内のみにシリコン酸化膜7を残存させる。

【0032】その後、半導体基板1上に熱酸化膜8とシリコン窒化膜9を順次堆積した後、ゲート電極の形成領域となるシリコン窒化膜9に開口部Bを形成し、半導体基板1全面に熱酸化を施した後、開口部Bを埋め込むように多結晶シリコン膜11を堆積する。次に、CMP法により、シリコン窒化膜9が露出するまで多結晶シリコン膜11を研磨して、開口部B内に、多結晶シリコン膜11からなるゲート電極12形状を形成する。

【0033】しかる後、熱燐酸溶液を用いたウエットエッチング法により、シリコン窒化膜9を除去することにより、素子分離手法に浅いトレンチ分離方法を使用することによって、従来のような素子活性領域（アクティブ領域）とフィールド領域との段差部分でのシリコン窒化膜のエッチング残渣等の問題がないので、シリコン窒化膜のオーバエッチング時のエッチング残りが生じない。そのため、寄生的に形成するFieldトランジスタのしきい値を低下させることもない。また、ゲート配線幅のバラツキを生じることがなく、断面形状のくびれ、或いはテーパー等の異常も生じない。

【0034】また、第2の実施形態に係る半導体装置の製造方法は、半導体基板1に浅いトレンチ分離層となる溝を形成する。半導体基板1全面にシリコン酸化膜6を形成して、溝内にシリコン酸化膜6を充填する。フォトリソグラフィ技術及びエッチング技術により、シリコン酸化膜6にゲート配線用の溝16を形成する。その後、前記溝16底部の酸化膜6を洗浄して除去する。

【0035】また、半導体基板1に熱酸化を施すことにより、溝16底部の半導体基板1表層にゲート酸化膜10を形成した後、開口部を埋め込むように多結晶シリコン膜11を堆積する。次に、CMP法により、シリコン酸化膜6が露出するまで多結晶シリコン膜11を研磨して、開口部内に多結晶シリコン膜11からなるゲート電極12形状を形成する。その後、シリコン酸化膜をエッチバックすることにより、シリコン酸化膜6からなる素子分離構造7を形成する。次に、素子分離手法に浅いトレンチ分離方法を使用することによって、シリコン窒化膜のオーバエッチング時のエッチング残りが生じない。

【0036】そのため、寄生的に形成するFieldトランジスタのしきい値を低下させることもない。また、ゲート配線幅のバラツキが生じなく、断面形状のくびれ、或いはテーパー等の異常も生じない。また、シリコン酸化膜6を用いて、埋め込みゲート配線を形成すると共に素子分離構造7を形成するので、埋め込みゲート配線形成の製造工程数を簡略化することが可能となる。

【0037】

【発明の効果】以上説明したように、本発明によれば、埋め込みゲート配線形成において、トレンチ型の埋め込み酸化膜を平坦化することにより、配線エッチング残りによる配線ショート、及びエッチングダメージをなくし、且つ、ゲート配線を寸法精度良く形成することが可能となる。

【図面の簡単な説明】

【図１】本発明の第１の実施形態に係る半導体装置の製造方法を示す製造工程縦断面図である。

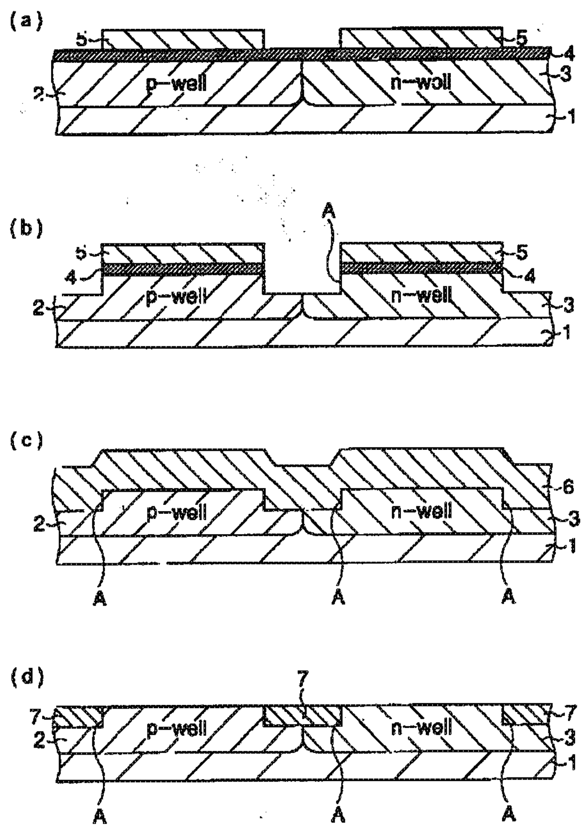
【図２】本発明の第１の実施形態に係る半導体装置の製造方法を示す製造工程縦断面図である。

【図３】本発明の第２の実施形態に係る半導体装置の製造方法を示す製造工程縦断面図である。

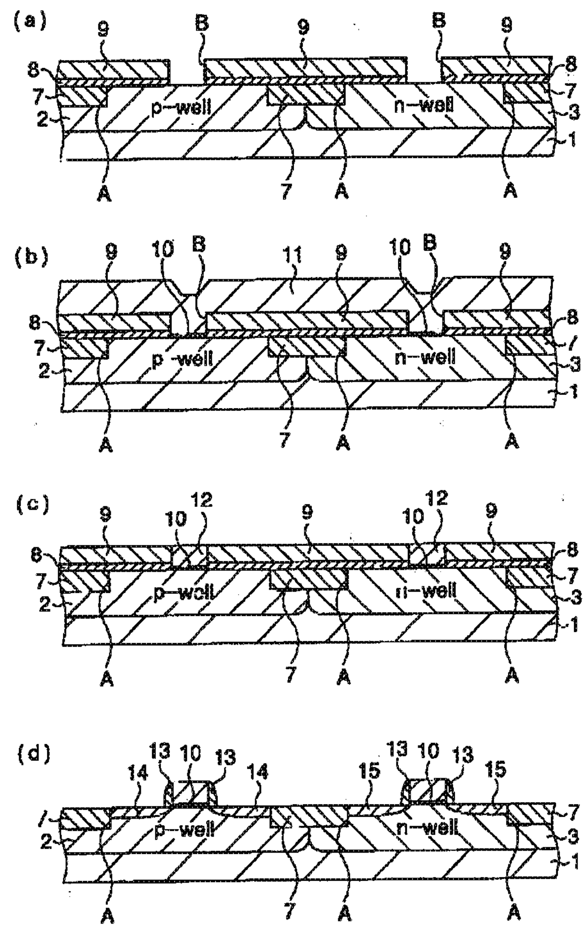
【符号の説明】

１　半導体基板
２　ｐ型ウエル
３　ｎ型ウエル
４　熱酸化膜
５　レジスト
６、７　シリコン酸化膜
８　熱酸化膜
９　シリコン窒化膜
１０　ゲート酸化膜
１１、１２　多結晶シリコン膜
１３　サイドウォール酸化膜
１４、１５　ソース・ドレーン
１６　溝

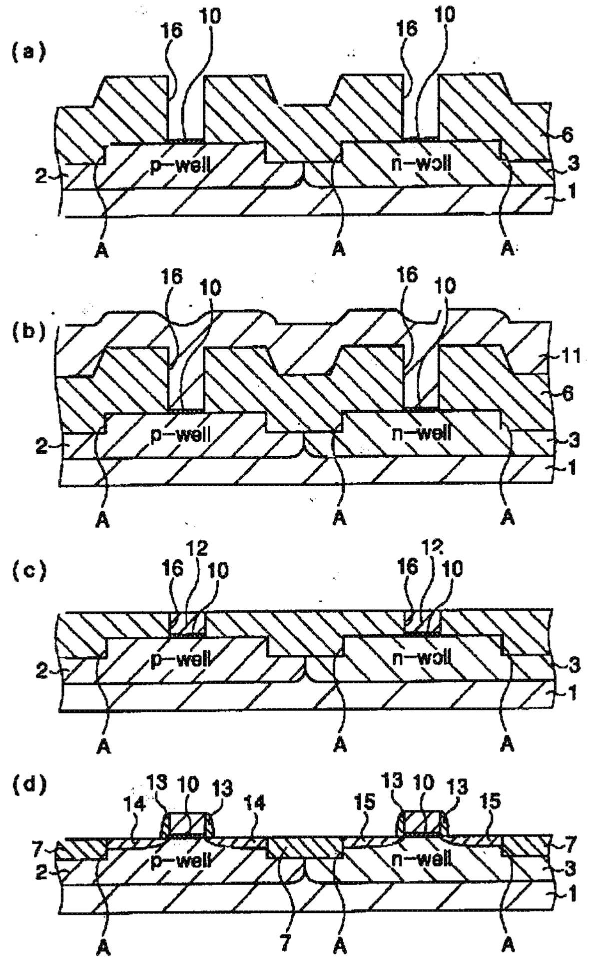
【図１】



【図２】



【図3】


(a)
16
10
16
10
p−well
n−well
6
3
2
1
A
A
A
(b)
16
10
16
10
11
6
p−well
n−well
2
3
1
A
A
A
(c)
12
16
10
12
16
10
p−well
n−well
2
3
1
A
A
A
(d)
13
10
13
14
14
13
10
13
15
15
7
7
2
p−well
n−well
3
1
A
7
A
A